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High-Performance Voltage Level Shifter Design Using TSMC 130nm CMOS Technology

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Abstract. Power-efficient integrated circuits often need to deal with differing voltages, so getting the voltages to shift properly and reliably is essential to get the signals to propagate correctly. In this paper, we present a design and implementation of a low-power, high-speed voltage level shifter that is specifically designed to be used with circuits for lithium-ion battery chargers. It was designed using TSMC's 130nm CMOS process technology and our simulations showed that it is able to shift voltages of 1.8V and 5V with a propagation delay of 0.09 ns. This design surpasses the previous ones, since they usually experience a delay of 0.15 ns. This shows that our proposed voltage level shifter is suitable for high performance VLSI systems with dynamic voltage operation.

1. Introduction

Level shifter (LS) circuit is one of the essential building blocks of a SoC. It enables communication between different chip components operating at different voltage levels. It ensures proper signal communication from the low-voltage side (V_{DDL}) to high-voltage side (V_{DDH}) and vice versa. A typical configuration is shown in Fig. 1, where a conventional level shifter (CLS) is implemented using 10 transistors. CLS is a synchronous device with two complementary inputs, V_{IN} and V_{INB} from the low voltage domain and V_Z is the output at the high voltage side.

If $V_{IN} = V_{DDL}$, then M1 turns on and pulls V_A node low, thus allowing M4 to charge V_Z to V_{DDH}. At this point, M2 is off because VGS of M2 is 0V (V_{INB} is low). However, a little fight is happening here. While V_{INB} is low, M4 keeps charging V_Z. As soon as V_{INB} goes high to V_{DDL}, M2 pulls V_Z low. This seems to be a little problem since M4 is in the middle of charging V_Z.

They seem to be pulling in different directions simultaneously.

This situation creates a certain friction between these opposing actions. As a consequence, it leads to even greater power consumption and even greater delays. This illustrates very well why traditional LS architecture is no longer viable. There have been several attempts to overcome the limitations of CLS. Zhai et al. [1], for example, employed a cascade arrangement of four CLS stages to amplify a 200 mV signal to 1.2V. However, incorporating such a solution requires the use of voltage regulators, which adds to the complication of the solution by increasing the circuit area and power consumption. However, the design in [2] achieved all this with just two CLS stages and, more importantly, without requiring any additional supply voltages, as the first stage was connected to a higher voltage by a diode-connected NMOS transistor.

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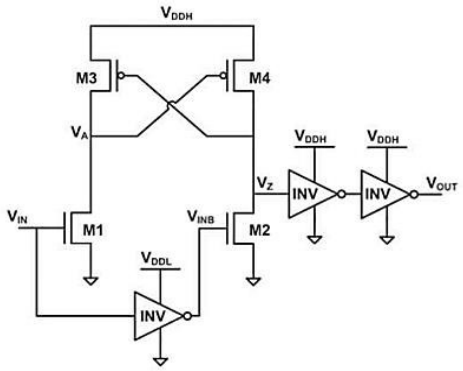


Fig. 1, Conventional cross-coupled half latch

This design isn't built for high-speed performance. So, there's a real need for a reliable, fast, and energy-efficient circuit to keep low-power designs strong and dependable. The design in [3] tried to improve the circuit by controlling the pull-up network's currents with a current mirror. While that gave it a wider operation range, but it also resulted in significant energy waste when the circuit remained inactive. Quiescent currents are defined as the amount of current that a circuit pulls from the battery when it is idle. Quiescent current is an important parameter for battery powered devices and low power electronics. When a device is inactive or when it is idle for a long time, it is extremely important to cut power drain. This is active power management and can save a lot of battery or power. The design in [4] is extremely admirable for this reason, as it bypasses this static current completely with the use of a level shifter with a Wilson current mirror.

This design is also impressive because it stops the flow of current whenever the desired output level is achieved, which is also a form of energy conservation. This is a great design, but it is a great design because it employs negative feedback, however, when this is done it requires some time to charge up the output node. This time gap can increase dynamic power consumption and result in slower speeds of signal transitions. When Vin is at a high value, the output node of the current mirror ends up floating. This strongly harms the output buffer performance. Some recent designs of current mirrors to correct these shortcomings are described. However, the modifications are minimal in furthering the objectives of reducing the delay and saving power, as noted in [5,6].

The current report is dedicated to the development of an energy-efficient voltage level shifting circuit built with a Wilson current mirror along with a gate driver. This component is used in battery charger chips. Our design is aimed at eliminating delay times while minimizing the chip area. Our improved level shift design is compared with other work in the literature [7,8]. As compared to other relevant work, the propagation delays are significant, and the maximum delays determine the speed at which the circuits operate. Therefore, in this work, we implement TSMC 130nm CMOS technology to design an improved level shifter with a 40% decrease in propagation delay, which enhances the speed of the circuitry. Additionally, the rise and fall times are similar, which contributes to the stability and reliability of the circuit. And occupies a significantly smaller area, measuring just 291.8799 um^2

2. Proposed Design

The section describes how we designed the level shifter. It includes the construction of the timing analysis to assure everything operates in an orderly fashion, and the selection process of the proper sizing of transistors. The target was to accomplish an ideal fast and efficient low power level shifter.

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2.1 Circuit Architecture

This study describes a design of a level shifter offering rapid operation speeds, power efficiency, and reliability in terms of switching domain voltage. The configuration, depicted in Fig. 2, consists of three primary components: a pre-driver stage, a logic block that mitigates cross-conduction, and a pull-up/pull-down output stage.

Two inverter gates whose purpose is signal refinement and level-shifting fast transitions from low 1.8 V logic levels are implemented into the pre-driver stage. There is an anti-cross conduction circuit in place to eliminate the possibility of both output transistors switching on simultaneously, which could lead to excessive current drain. The circuit includes an AND gate and a set of active transistors that ensure the two transistors don't simultaneously bias on, thereby shielding the circuit from shoot-through current. Transistor M2 (HV_PMOS) and transistor M5 (HV_NMOS) form the pull-up/pull-down output stage, which enables the output node, OUT_VCC, to change states between low and high, maxing out at 5 V.

The primary components involved in level shifting are M4, M7, M8, M11, along with the resistor R0 and the capacitor C0, all of which are responsible for pulling the intermediate nodes up and down. Transistors M 4 and M 7 are NMOS and discharge the nodes. M8 and M11, PMOS, are responsible for pulling up the nodes. Changing the input from high to low is a process C0 helps with by discharging the Vg11. This process activates M8, which raises the level of the node Vg5. Conversely, the transition from low to high activates M7, which pulls the node Vg5 down, thereby deactivating M8. Between Vg5 and DGND there's a diode, D0, which works to protect M5 from negative gate-to-source voltages during switching and when DGND rises more quickly than Vg5.

Each section of the circuit uses a different power supply. The logic section uses the V1P8 power supply at a value of 1.8 V, and the output section uses the VCC power supply at 5 V. The M2, M8, M5, and M11 transistors are required to be high- voltage ones due to the full 5 V the transistors need to withstand. If, however, there are lower voltage transistors, then M7 needs to be sized 20 times larger than normal in order to be able to switch properly. The large size of M7, however, must be built at the expense of the chip as it is able to slow down the circuitry and cause an increase in the power usage of the circuit.

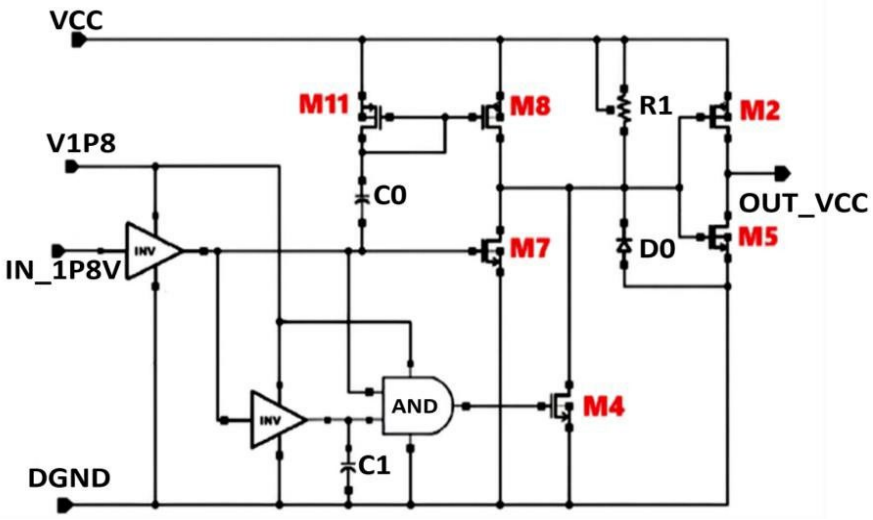


Fig. 2 The circuit diagram of developed Level-Shifter under cadence tool version

After showing how the level shifter is built and how its transistors are arranged, we then look at how well it works in real time. The main thing we're interested in is the propagation delay, which is really important when it comes to changing voltage levels smoothly and quickly.

2.2 Propagation Delay Analysis

Propagation delay refers to the amount of time it takes for a signal to travel from the beginning of a circuit to the end of the circuit. For level shifters, it is preferable to have a lower delay. Lower delays allow switches to be executed faster and with more dependability, especially with large gate capacitances associated with power transistors.

There are a couple factors that determine the propagation delay T_P. To start off, the total load capacitance that the switching node will have to manage is a factor. Secondly, the drive current of the transistors is a factor, as it determines how efficient the transistors will be at moving the charge. Another factor is the overdrive voltage, which is the discrepancy between the gate-to-source voltage (Vgs) and the threshold voltage (Vth). Lastly, the delay will be impacted by the specific technology that is utilized, including different attributes such as mobility (μ_n) and oxide capacitance (Cox). These factors are all correlated with one another, and the relationship between the factors can be stated with a circuit propagation time equation:

$$T_P = \frac{C_{total}}{I} \tag{1}$$

The sum total capacitance C_{total}, which includes the gate capacitances of the driven transistors (M2 and M5) as well as parasitic capacitances along the level shifter path which are derived from interconnections and intrinsic capacitances. When transistors are fully turned on and operating in saturation, the current can be expressed as the following:

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - Vth)^2 \tag{2}$$

When we plug Eq. 1 into Eq. 2, we get:

$$T_P = \frac{C_{total}}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-Vth)^2} \tag{3}$$

This illustrates that as a transistor's width increases and the gate voltage is elevated further over some threshold, the duration that a signal takes to propagate decreases. These are things that we can manipulate by changing the size of the transistors. On the contrary, increasing the channel length and/or adding more capacitance results in longer propagation delays. Thus, in your design, there is a need to find a suitable trade-off between the aforementioned to achieve optimal results.

2.3 Transistor Sizing and Optimization

Designing high-speed and low-power level shifters requires choosing appropriate transistor sizes. Each transistor's dimensions influence the delay and reliability of the circuitry. More specifically, the dimensions of each transistor influence the rate at which the intermediate nodes charge and the rate at which they discharge. This, consequently, affects the circuitry's speed and power usage. The selected dimensions of the optimistic transistor of the level shifter are shown in Table 1.

Table 1. Sizes of the components for the optimized level shifter

Transistors Names	Length	Width
pch_tgo5_mac (M2, M8, M11)	500 [um]	1.9 [um]
nch_tgo5_mac (M5)	600 [nm]	740 [nm]
nmos1v_mis (M4, M7)	130 [nm]	2 [um]
nmoscap_tgo5 (C0)	2 [um]	2.5 [um]
nmoscap_tgo5 (C1)	1.6 [um]	2.5 [um]
rppolyhri_dis (R0)	2.7 [um]	400 [nm]
ndio_tgo5(R0)	940 [nm]	740 [nm]

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The transistors for the level shifter, M4 and M7, are assigned the shortest channel length and a reasonable width for the task, 130 nm and 2 µm, respectively. This configuration optimizes the trade-off between speed, area, and robustness. In comparison, the high-voltage transistors (M2, M5, M8, M11) are designed for 5 V. M2, M8, and M11 are designed for long channels for added reliability, and M5 is designed with a volume increase to ensure that large capacitive loads are handled without compromising timing.

Dimensions of the transistors were selected to optimize the trade-off between speed, area, and robustness. The design also needs to consider that aggressively shrinking the width of the transistors, to save the layout space, also incurs costs. For example, if the width is too small, a design with only a single contact for the source and drain may end up being proposed. This situation is usually avoided because it results in increased resistance, and reliability may also be lacking. It is important to design a transistor that strikes a trade off between the speed of the circuit, the amount of space it occupies, and manufacturability.

3. Simulation results and Discussions

After thoroughly adjusting the sizes and optimizations of the transistors, this section demonstrates the simulation results, discusses some details regarding the incorporation, and makes a comparison to determine the effectiveness of the suggested level shifter. All simulations were performed using Cadence Virtuoso TSMC 130 nm CMOS technology.

3.1 Transient Analysis of the Proposed Level Shifter

Fig. 3 shows the results of a quick simulation that successfully shifts the logic level from 1.8 V up to 5 V. The measured delays for signal propagation are:

- tp1 = 0.09005 ns (low-to-high transition)
- tp2 = 0.09112 ns (high-to-low transition)

These almost identical numbers show that the circuit switches in a balanced way and works reliably.

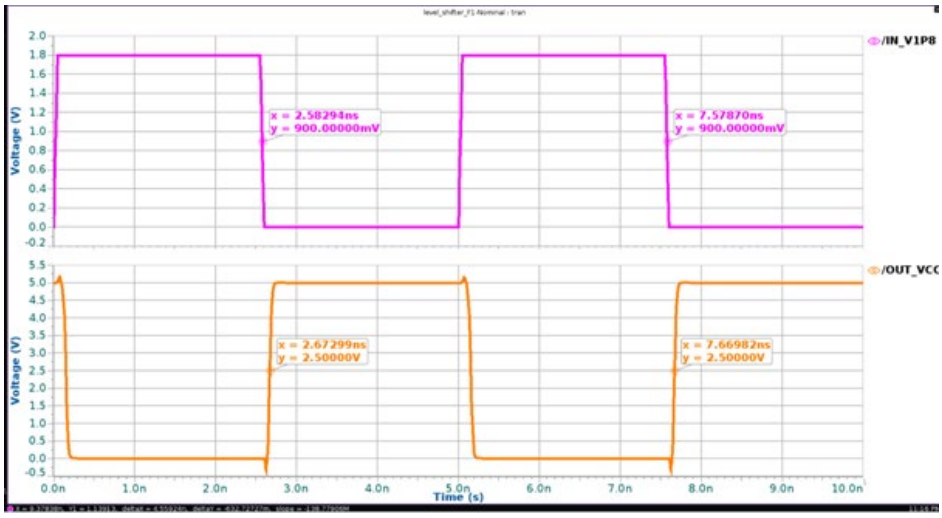


Fig.3 Transient Analysis result of the Proposed Level-Shifter

3.2 Comparison with Literature:

After performing the simulations, we compared the outcomes of our design to other recent works. In Table 2, we present the tech nodes, ranges of voltages and the time delays. Using the 130 nm CMOS tech for our design, we achieved a record breaking propagation delay time of 0.09 ns which also outranged other designs with different tech nodes. For example, Alaoui and co. [7] did a 180 nm process and recorded 0.15 ns delay, but we had a better time. On the other hand, Zhao et al.

M8 with a smaller tech of 130 nm, had a much worse time of 1.51 ns. In even more advanced tech, Shukla et al. M9 with 65 nm also had a better time of 0.63 ns and for 7 nm, Saurab and Chavan [10] 1.88 ns. Gosatwar et al. [11] with 90 nm did the worst with 10.99 ns. Chatterjee et al [12] also did worst at 28 nm with 3.11 ns.

These results suggest that merely shrinking the technology does not instantly lead to better results. Getting the highest performance in your circuits requires precise adjustments and clever design techniques.

Table 2. A Comparison of the proposed level shifter with previously reported designs

Design	Technology	Low Voltage	High Voltage	Delay Time
Proposed Design	130[nm]	1.8[v]	5[v]	0.09[ns]
Alaoui *et al* [7]	180[nm]	1.8[v]	5[v]	0.15[ns]
Zhao *et al* [8]	130[nm]	1.8[v]	5[v]	1.51[ns]
Shukla *et al* [9]	65[nm]	1.2[v]	6[v]	0.63[ns]
Gosatwar *et al* [10]	90[nm]	0.2[v]	1[v]	10.99[ns]
Saurab *et al* [11]	7[nm]	0.19[v]	1.5[v]	1.88[ns]
Chatterjee *et al* [12]	28[nm]	2.25[v]	1[v]	3.11[ns]

3.3 Post layout simulation:

Once an integrated circuit has been designed, the next task is the layout, where the plan of the circuit is etched on an extremely small piece of semiconductor material. At this point, all the details are completed as engineers place and connect the components of the layout according to the design. This process starts with floor planning, where the outline of the circuit is drawn and its overall shape and size are determined. After this, individual circuit components are placed, one by one, with consideration of the function of the components placements on the circuit as well as the arrangement in order to facilitate good signal flow. Once all components are on the layout and all placements are optimized, you connect the components of the circuit by drawing the electrical routes. At this point, you should adjust the width and the spacing of the routes as well as the distances between connections while trying to avoid problems with electromigration. Electronics routing is critical in achieving seamless performance of the circuit by maintaining high routing speeds and clear signals.

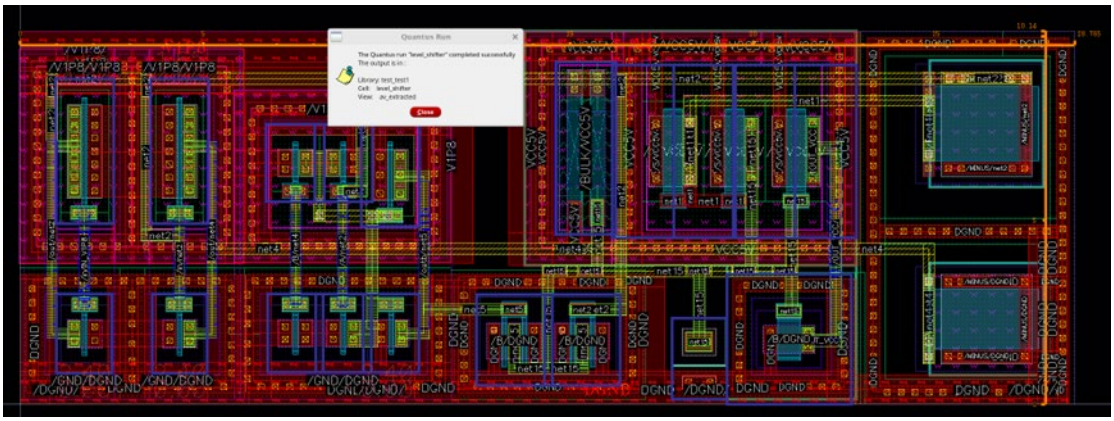


Fig.4 The layout of the proposed Level-Shifter

For the most part, the arrangement complies with various standards and undergoes numerous inspections and simulations to ensure it fulfills all design requirements, production constraints, and operational requirements (such as DRC, DFM, MRC, antenna, density, and LVS). The total area occupied by the arrangement is around (10.14 um ×28.785 um).

Once the routing and layout of our circuit are complete, a post-layout simulation is performed to verify that the extracted layout accurately reflects the intended design, while taking into account implementation-related effects. The results of this simulation, illustrated in Fig. 5, demonstrate the performance of the proposed level shifter. The measured propagation times are tp1 = 0.09379 ns for the low-to-high transition and tp2 = 0.09488 ns for the high-to-low transition.



Fig.5 Post-layout simulation result of the Proposed Level-Shifter

The post-layout simulation results closely match the layout results, with a minimal increase in propagation time (approximately 3 to 4 ps). This small variation indicates that we have a negligible impact on performance, thus confirming the accuracy and robustness of the implementation design.

Conclusion

This paper describes an updated custom voltage level shift, optimized to minimize delay and improve performance of an overall system. The focus of the study was the newer implementation of classic designs that improved performance from 0.15 ns of delay to 0.09 ns, and cutting it to 40% of the delay measured. This shift was tested in the 130 nm technology provided by TSMC, and the simulations of the circuits were designed in the Cadence Virtuoso environment. The simulations showed the classical designs were reaching the performance expected of state of the art level shifters used in charging high performance batteries and were incorporating optimum functionality expected in a complete System-on-Chip (SoC).

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