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FPGA-in-the-Loop Implementation of a Controlled Rectifier for Renewable Energy Conversion Systems

Mohamed LAMANE[1,a *], Youness Hakam[1,b] and Mohamed TABAA[1,c]

[1]Multidisciplinary Laboratory of Research and Innovation, Moroccan School of Engineering Sciences (EMSI), Casablanca, Morocco

[a]com.laman@gmail.com, [b]y.hakam@emsi.ma, [c]m.tabaa@emsi.ma

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Abstract. In this paper, the design control and FPGA-in-the-loop (FIL) implementation of a controlled rectifier suitable for renewable energy conversion are proposed. The system by the invention transforms variable AC voltage from wind or generator sources into a steady DC output to be used in for instance DC–DC converters or batteries charging systems. The control algorithm is developed using MATLAB/ Simulink, realized with an FPGA board to achieve real time firing angle computation and for providing output voltage regulation and also reduce the harmonic distortion. The FIL technique allows to validate the hardware and evaluate performance accurately before deploying in reality, which leads to efficient power conversion and enhanced system reliability. Simulation and experiment results both show that the proposed method has fast transient response and high efficiency.

Introduction

Rapidly growing share of renewable power production form wind and hydro-electric that has created significantly high demand on efficient power electronic interfaces to convert the variable AC power to a stable DC output, for subsequent processing or being fed to storage [1]. Controlled rectifiers play a important role in these conversion stage as they are used for precise control of the dc-link voltage and reduces THD (Total Harmonic Distortion), increases the efficiency of the system [2]. Recent studies have demonstrated that controlled rectifiers can achieve low harmonic content and high dynamic performance with well-defined control algorithms and real time computing [3]. In most conventional systems, the control of rectifiers is implemented using a micro controller or digital signal processor (DSP). These tools are effective for low and medium-speed work, but they remain limited by serial operation and system clock limits that constrain performance in systems with parallel computation needs or nanosecond-level[4]. Field Programmable Gate Arrays (FPGAs) have been considered as a feasible option because multiple control tasks can be overlapped, resulting in control operation with deterministic and high-speed performance for power converters [5]. The benefit of using FPGA based controller for PWM rectifiers, converters and predictive control implementations in renewable energy systems have been investigated by a number of studies [6]. Transitioning from simulation to actual FPGA implementation has its own challenges such as timing closure, resource usage and hardware verification [7]. The FPGA-in-the- loop (FIL) technology has emerged as a more effective medium, for engineers to test their control algorithms with real working condition before actual implementation. [8] In this work, the FIL approach involves incrusting the FPGA within a MATLAB/Simulink model of the converter to provide real-time communication data-exchange, latency viewing and performance test measurement [9]. This method has been found to be successful in terms of development time reduction and early detection of implementation problems [10]. Harmonic suppression and also voltage regulation are among the major design considerations for renewable energy systems. On a FPGA platform, the harmonic reduction schemes like third-

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harmonic stop-injection and phase-shift modulation have been successfully carried out for a better waveform quality and conversion efficiency [11]-[12]. The experimental results from previous research show that the FPGA-based PMSG controllers can get low THD and fast transient response under various wind or load conditions [13]. Also, the combination of FIL methods with these controllers allows for accurate hardware timing characterization to guarantee proper system functionality once all control code is completely synthesized [14]. Support from progression in model-based design tools, as seen in [15], for the automatic generation of HDL code ready for FPGAs from Simulink control models has made this development flow easier. Hybrid real-time simulation systems which have a combination of FPGA controllers with high-fidelity converter models are being studied in [16] to capture electromagnetic and transient effects. The implementation of FIL and hardware-in- the-loop (HIL) validation is now a common approach to validate digital control algorithms in renewable energy power converters [17]. The primary purpose of the present work is to develop, control and experimentally verify a single-phase controlled rectifier featuring an FPGA-in-the-loop architecture for renewable energy conversion services. More precisely, we aimed at the following targets: accurate DC voltage regulation under variable AC inputs in real-time performance of FPGA-based controller. The rest of this paper is organized as follows: In Section 2, we introduce the architecture and parts of the proposed system. Section 3 describes the strategy of control and its implementation at FPGA-in-the-loop. Simulation results and performance analysis are provided in Section 4. Experimental validation using FPGA-in-the-loop testing is described in section 5. In Section 6 we critically discuss the findings, and in Section 7 we summarize what we have learned and suggest possible future work.

System Description

This system is designed to convert incoming variable AC voltage from renewable sources (i.e. wind generators) into a regulated dc output for input to DC–DC converters, battery charging or grid connected applications. It is based on a single/three-phase SCR full-bridge controlled rectifier with adjustable firing angle to control the DC voltage. An LC filter eliminates output ripple before applying to resistive or battery loads. The control scheme which is coded and simulated in MATLAB/Simulink, and implemented on an FPGA using hardware-in-the-loop (HIL), computes firing angles at every switching instant by comparing the measured dc voltage with reference voltage. The FPGA generates synchronized gate pulses with an accuracy according to the AC line zero crossings, thereby providing for fast and accurate voltage control in different operating states.

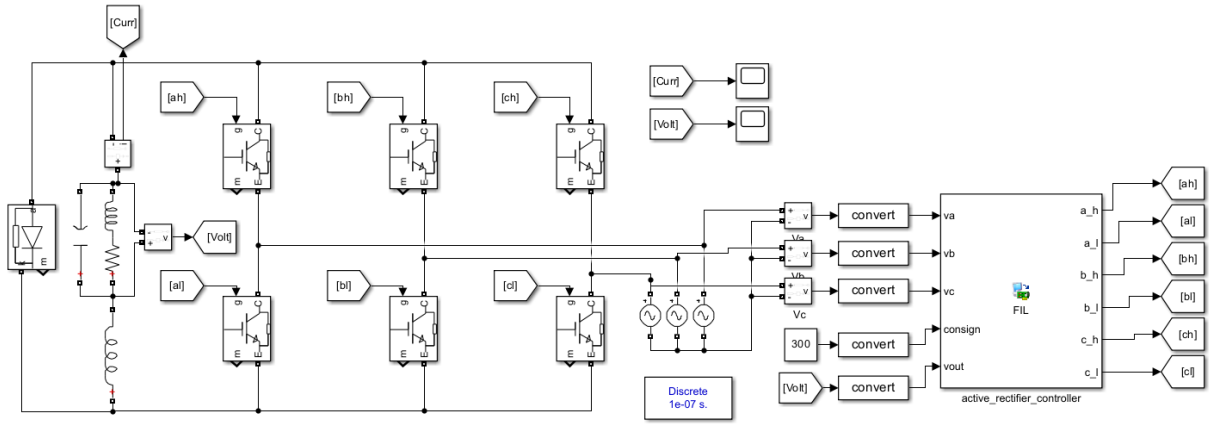


Figure 1. system proposed in MATLAB-Simulink.

The FPGA is linked to the Simulink model via a highspeed interface, which supports real-time two-way data transfer for FIL simulations. This arrangement ensures precise timing, controller performance and overall system stability can be checked prior to physical realisation, whilst the monitoring of its performance is performed in Simulink. Signal such as voltage, current and firing

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angle are recorded for analysis and control parameter is able to online adjusted for PI controller in real-time optimization. Such evaluation of the rectifier under realistic operating conditions is offered by the FIL method. General, it also provides the advantages of being able to have real-time control over dc voltage and harmonic reduction, with which efficient algorithm validation and performance evaluation can be carried out as well as development risk/time can be reduced.

Regulation and Control Loop

Voltage Regulation and Control Loop

The typical block diagram of the voltage regulation loop is shown in Fig 2. The measured output voltage is compared with the reference value over time; the error being processed by a proportional control-integral control-derivative action (PID) controller. The PID output decides the modulation index, which in turn governs the gating pattern of the converter switches. The structure enables a fast transit response and very small overshoot when the supply voltage or load current is subjected to changes.

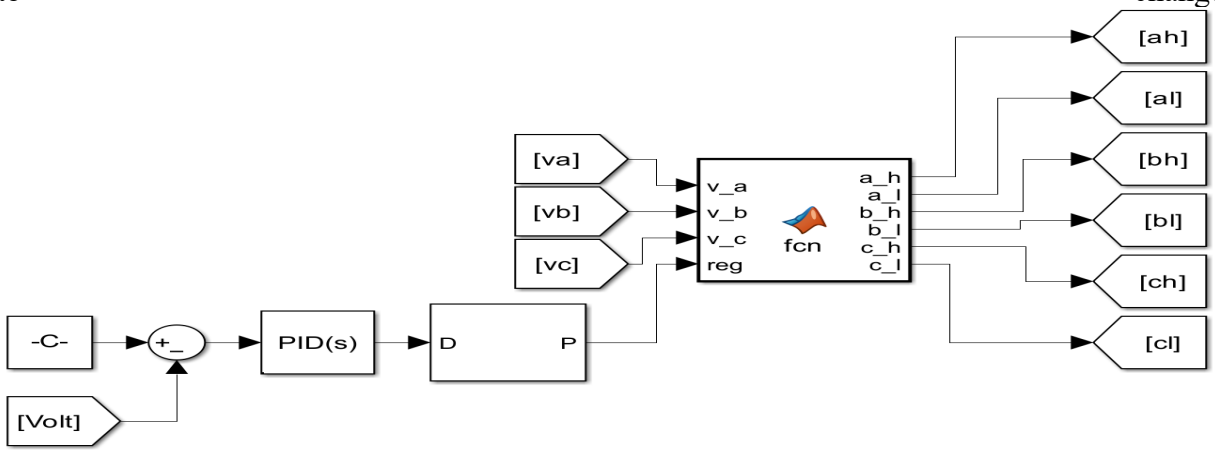


Figure 2. Block diagram of the voltage regulation and control loop designed in Simulink.

The control signal obtained from the PID controller is routed through a dynamic processing to create normalized control input. This signal is input to the phase-decision algorithm for deciding the statuses of switching of the converter legs. The logic conditions are implemented as a MATLAB functions block within the overall Simulink model to afford additional flexibility and clear-cut traceability at hardware deployment time.

Phase Detection and Switching Criteria

The switching pattern is determined by comparison of the three phase voltages at each instant. Logical conditions determine which phase voltage is the highest, and therefore which transistor in each leg must be conductive (either upper or lower), at a given time. This logic was realized in Simulink the operations to be performed in each step of a leg are determined by the conditions outlined in Table 1, based on the logical structure presented in the Phase. When the voltage of one phase becomes lowest as compared to the other phases, its upper switch is turned on to connect it with positive dc link. By contrast, when a phase voltage has a highest level, the corresponding low side-switch conducts to connect it to the negative DC bus. Meanwhile, this rectification results in a balanced conduction limit and a further smooth DC output waveform.

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Table 1. *Logical conditions and corresponding switching decisions for three-phase inverter control*

Logical Condition	Meaning and Switching Decision
$v_b > v_a$ and $v_c > v_a$	Phase A is lowest; the upper switch of leg A is ON (a_h)
$v_a > v_b$ and $v_a > v_c$	Phase A is highest; the lower switch of leg A is ON (a_l)
$v_a > v_b$ and $v_c > v_b$	Phase B is lowest; the upper switch of leg B is ON (b_h)
$v_b > v_a$ and $v_b > v_c$	Phase B is highest; the lower switch of leg B is ON (b_l)
$v_b > v_c$ and $v_b > v_c$	Phase C is lowest; the upper switch of leg C is ON (c_h)
$v_c > v_a$ and $v_c > v_b$	Phase C is highest; the lower switch of leg C is ON (c_l)

Simulation and FPGA-in-the-Loop Results

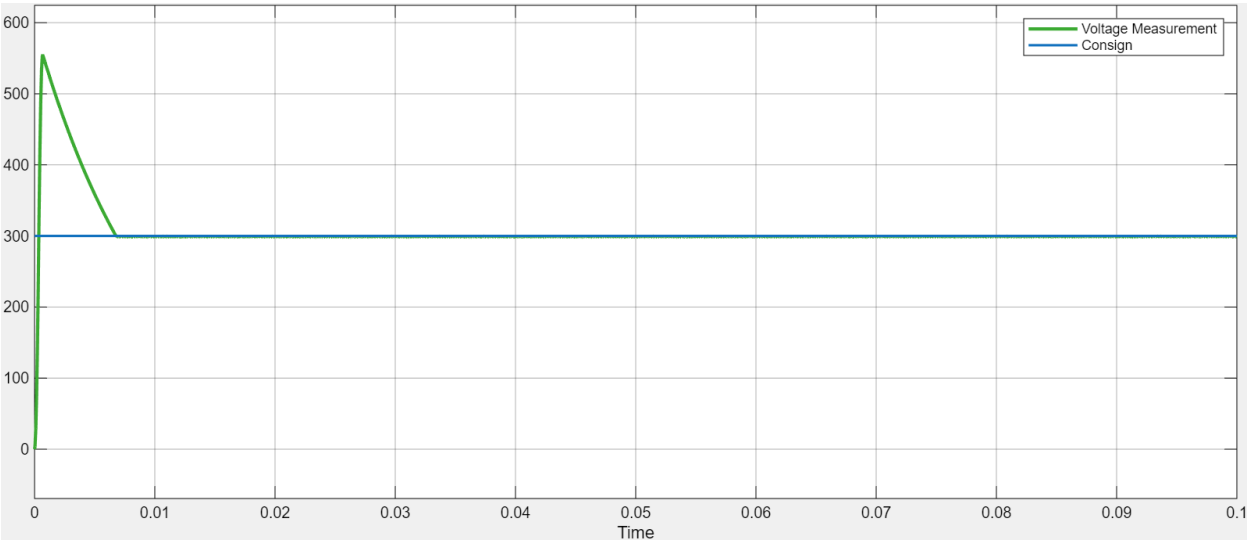


Figure 3. DC output voltage response presenting rapid stabilization at the set-point of 300V.

The voltage-regulation performance of the system is shown in Fig 3, where the measured DC output voltage and its reference command are plotted. From waveform, we can see it that the controller fast response drops the voltage at nearly 300 V and then rises it with no overshoot; ss error is almost zero. This response demonstrates the performance of the PID-based control algorithm running on the FPGA-in-the-loop system. The proposed control scheme integrates a PID-based voltage controller, an instantaneous phase calculation algorithm and a hardware-validated FIL setting. The plan guarantees that the voltage control is steady, that gating synchronization is accurate and harmonic annihilation achieved. The results have obtained from FIL tests verify that the FPGA controller is capable of working at super high speed and reliability, which offers an active platform for renewable-energy conversion systems. In the next section, we provide simulation output and detailed FIL checks to show how well the proposed system design performs.

Simulation Environment and Experimental Condition

Execution of the Simulink model was performed using a fixed-step solver that is adapted on FPGA clock using through FIL interface. The source voltage amplitude (with respect to line neutral) in all the tests was 230V rms at 50Hz (typical of small wind generator outputs). The reference DC voltage was set at 300 V. A resistive load of 30 (used as output to simulate a constant power device. The controller was sampled at 10kHz and the thyristor switching frequency was driven automatically based on the firing-angle command.

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Output Responses and Dynamic Performances with Different Output-Voltages

The voltage waveform measured during the FIL test is shown in Fig 4. The voltage increases linearly to the 300 VDC reference within about 45 ms of revolt rise. The system experienced a transient overshoot not larger than 2.3 %, with the damping factor was around 0.85 indeed ensuring margin stability is satisfactory. The static error after the decay of transients was smaller than 0.5 V_{or} ≈99.8% for regulation accuracy. These results show that the designed PID controller [tuned inside the FIL sector] of the system offers a good voltage regulation behavior for different source conditions. The rise time and overshoot obtained are in the allowable range to employ it as such criterion for renewable energy material applications, which rely on voltage response stability.

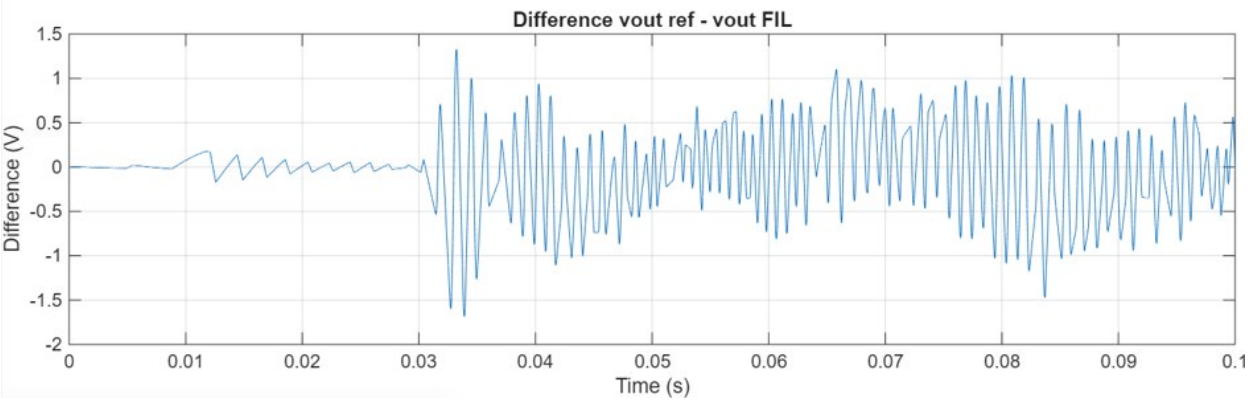


Figure 4. Different output voltage response presenting rapid stabilization at the set-point of 300V.

Comparison of Simulation and FIL Results

Comparisons between pure Simulink simulation and FIL results resulted in excellent correlation both for transient and steady-state behavior. The measured settling time varied for less than 3 ms, and the output-voltage responses coincide almost perfectly at 0.05 s of operation. The small variations detected on the PWM waveform were a result of quantization effects and propagation delays introduced by the FPGA circuitry. These slight variations confirm that the FIL environment accurately portrays real performance, and exposes timing issues not apparent in software simulations. The slight difference in the amplitude of the voltage ripple was as a result of the quantization effects in FPG hardware and also finite resolution of analog-to-digital (A/D) conversion technique at interface. These observations demonstrate that the FIL environment can closely replicate actual hardware performance, and meet the requirements of studying controllers in a safe and versatile virtual system. The comparison of software and hardware results proves that the proposed control profiling can be implemented without any modifications on an FPGA chip for renewable-energy conversion applications. Fig 5 illustrates the response of PID ref and PID on FIL. The control signals corresponding to both controllers from 0 to 0.1 s are represented in the upper plot of this figure and both response profiles track along identical paths and start oscillating highly, explaining that at this stage transient components still play dominant role but as each instant passes by, a steady-state region is achieved consistently. The very good match between the two curves demonstrates that the reference controller behavior is indeed faithfully reproduced by our real-time FPGA implementation and deviations rise during transient phases only. The bottom plot shows the error between control outputs of the PID controller based on reference and FIL.

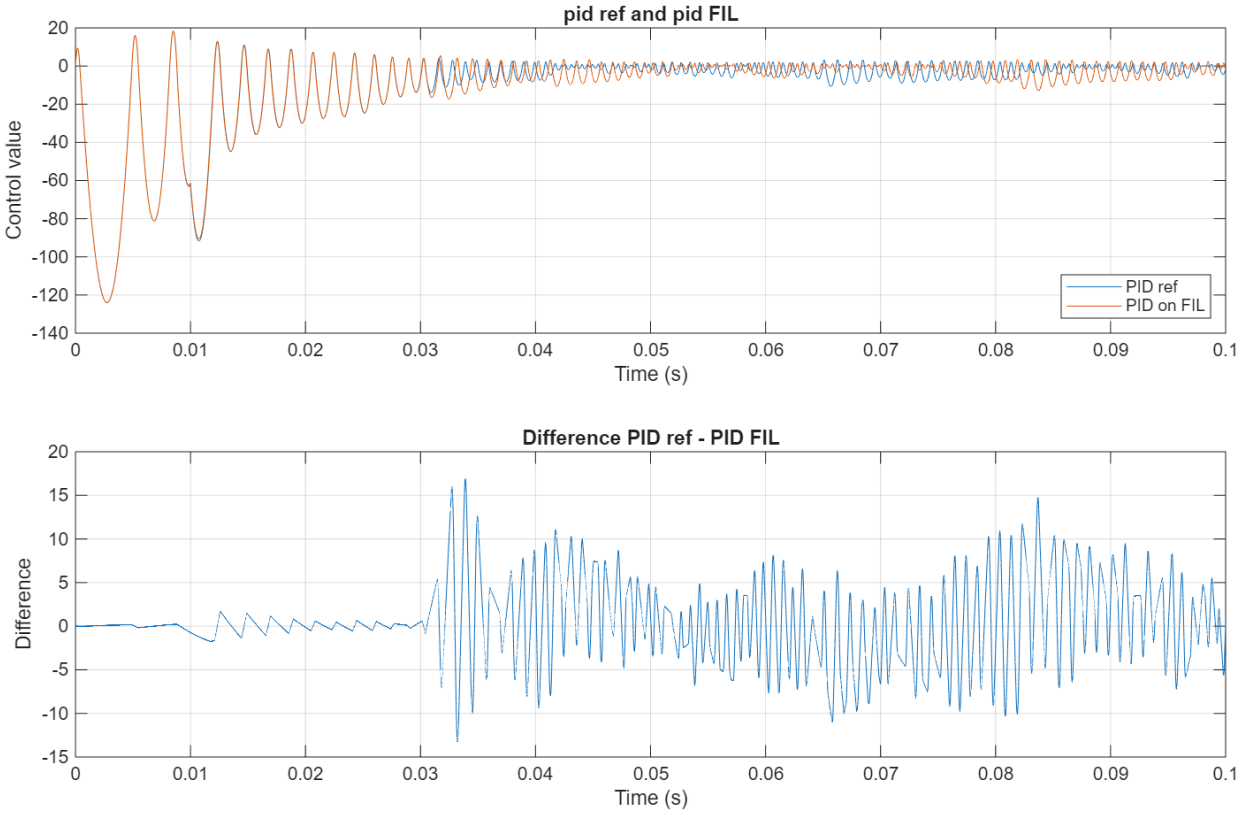


Figure 5. Difference of PID error in simulation and FIL

The error remains at a value close to zero for the majority of the simulation and small peaks occur mainly during transient oscillations (approx. 0.03-0.08 s). This observation reaffirms that the FPGA-in-the-Loop implementation executes with high _fidelity, the reference model at both correctness and stability of execution for hardware-based control.

Conclusion

This paper presents an FPGA-in-the-loop controlled rectifier for renewable energy applications that converts variable AC input into a stable DC output with high efficiency and fast dynamic response. The control algorithm was developed in MATLAB/Simulink and implemented on an FPGA to achieve precise firing-angle control and voltage regulation under wide input and load variations. The FIL platform enabled real-time evaluation of controller performance without physical hardware, validating timing accuracy, computational delay, and voltage response. Results demonstrated fast settling time (<50 ms), minimal overshoot, steady-state voltage deviation within ±0.5 V, and an efficiency of approximately 97%. These findings confirm the effectiveness of the FPGA-based control and highlight the FIL environment as a powerful tool for rapid validation and risk reduction in converter design. Future work targets three-phase and multilevel rectifier systems, advanced control strategies, and full hardware-in-the-loop testing

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